PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re United States Patent Application of:		**Docket No.:**	**2771-497 (7486)**
Applicant:	**STAUF, Gregory T., et al.**	**Examiner:**	**Thao X. LE**
Application No.:	**09/681,609**	**Art Group:**	**2814**
Date Filed:	**May 8, 2001**	**Confirm. No.:**	**8601**
Title:	**BARRIER STRUCTURES FOR INTEGRATION OF HIGH K OXIDES WITH Cu AND Al ELECTRODES**	**Customer Number**	**25559**

EXPRESS MAIL CERTIFICATE

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Candace White

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APPEAL BRIEF
IN U.S. PATENT APPLICATION NO. 09/681,609

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This Appeal Brief is filed in support of the appeal initiated by Notice of Appeal filed November 18, 2003 in U.S. Patent Application No. 09/681,609, appealing from the final rejection of claims 1-39 in the May 19, 2003 Office Action.

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This Appeal Brief is submitted in triplicate copies.

An oral hearing is not requested.

REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Technology Materials, Inc., 7 Commerce Drive, Danbury, CT 06810. Such party is the owner of the invention and patent rights of the present application by virtue of an assignment from the inventors Gregory T. Stauf, Bryan C. Hendrix, Jeffrey F. Roeder, and Ing-Shin Chen, as recorded in the assignment records of the U.S. Patent and Trademark Office on July 26, 2001 at Reel 012012, Frame 0409 (3 pages).

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellants, appellants' legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-39 are pending in the present application and are the subject of this appeal.

Claims 1-26 and 28-39 has been finally rejected in the May 19, 2003 Office Action. Claim 27 was found to prospectably allowable if re-written in independent form and was rewritten in the Amendment filed on November 18, 2003.

A copy of the appealed claims 1-39 is attached in **Appendix A** hereof.

STATUS OF AMENDMENTS

No amendments have been made to the claims 1-26 and 28-39 subsequent to the issue of the May 19, 2003 Office Action finally rejecting such claims.

The prospectably allowable claim 27 was first rewritten into independent form in a Response filed on August 19, 2003. The Examiner denied entry of the August 19, 2003 Response, on the basis that claim 27 was not rewritten in proper form, i.e., it failed to incorporate all limitations of the base and intervening claims therein.

In an Amendment subsequently filed on November 18, 2003, claim 27 was for the second time rewritten into independent form, by incorporating all limitations of the base and intervening claims therein, consistent with the Examiner's requirement. However, to this date, the Appellants have not yet received any communication from the Office regarding either entry of or refusal to enter the November 18, 2003 Amendment.[1]

Because the November 18, 2003 Amendment complies with the Examiner's requirement and is enterable udner 37 C.F.R. 1.116 (b), claim 27 in the attached listing of claims is set forth in its rewritten independent form as amended in the November 18, 2003 Amendment.

SUMMARY OF THE INVENTION

Appellants' claimed invention is a microelectronic structure comprising at least one conductive barrier layer between a layer of high dielectric constant material and a metal layer comprising Cu or Al, which can function as a Cu or Al electrode.

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[1] A telephone call was made to Examiner Le on January 13, 2004 concerning the status of the November 18, 2003 Amendment; Examiner Le stated that the November 18, 2003 Amendment had not reached the Examiner until January 5, 2004 and has not yet been reviewed by the Examiner.

Complex metal oxides such as $SrBi_2Ta_2O_9$ (SBT), $(Ba,Sr)TiO_3$ (BST), and $Pb(Zr,Ti)O_3$(PZT), which are characterized by high dielectric constants, are particularly suitable for forming integrated capacitors of high capacitance.

However, usage of such high dielectric constant materials require electrodes made from noble metals, noble metal alloys, or noble metal oxides, etc., which are expensive and difficult to process. They are further disadvantaged by their relatively low conductivity.

Aluminum and copper electrodes, on the other hand, not only are cheap and easy to process, but also have excellent conductivity. However, aluminum and copper electrodes are vulnerable to oxidization and are difficult to use in combination with high dielectric constant metal oxides.

Appellants' claimed invention solves the above-described problem by providing a conductive barrier structure between the high dielectric constant material and the aluminum or copper electrode.

Specifically, the claimed microelectronic structure, as recited by claim 1 of the present application, comprises:

at least one layer of high dielectric constant material (see page 6, lines 11-17 of the instant specification);

at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from

the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof (see page 7, lines 9-14 and page 13, lines 1-18 of the instant specification);

at least one metal layer in contact with the conductive barrier layer, wherein such metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al, with the limitation that when the at least one metal layer material is Al, the at least one conductive barrier material is not Ir or IrO_2 (see page 6, lines 8-10 and page 7, lines 15-19 of the instant specification); and

wherein the at least one conductive barrier layer is between the at least one layer of high dielectric constant material and the at least one metal layer (see page 6, lines 9-11 of the instant specification).

The at least one metal layer of Appellants' claimed invention thus provide a metal electrode that comprises Cu, Cu alloy, Al, Al alloy, or other combinations of metals that contain Cu and/or Al (see page 8, last paragraph, and page 9, first paragraph of the instant specification).

The conductive barrier structure of the present invention may comprise two or three barrier layers, as recited in claims 18-26 and 28 of the present application and disclosed on page 8, lines 3-6; page 9, lines 4-18; and page 10, lines 1-5 of the instant specification).

Further, Appellant's claimed invention encompasses various conductive barrier structures that are particularly suitable for protecting a metal layer that comprises Cu or Cu alloy from high

dielectric constant BST, SBT, BT, or PZT material layers, as recited in claims 28-31 and disclosed on pages 10-12 of the instant specification.

Appellants' claimed invention therefore provides effective conductive barrier structures for protecting Cu- and/or Al-containing metal electrodes from high dielectric constant material layers.

ISSUES

The issue presented in this appeal are:

(1) Whether claims 1-8, 11-12, 14 and 16-17 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Tsu et al. USP 6,294,420 (hereafter "Tsu");

(2) Whether claims 1-10 and 18 are unpatentable under 35 U.S.C. §103(a) as being obvious over Lu et al. USP 6,365,517 (hereafter "Lu") in view of Tang et al. USP 6,462,931 (hereafter "Tang"); and

(3) Whether claims 13, 15, 18-26 and 28-39 are unpatentable under 35 U.S.C. §103(a) as being obvious over Tsu in view of Tang.

GROUPING OF CLAIMS

For each ground of rejection set out in the preceding section ("ISSUES"), the representative claim is identified below.

(1) Rejection of claims 1-8, 11-12, 14 and 16-17 under 35 U.S.C. §102(e) as being anticipated by Tsu - Claim 1 is representative.

(2) Rejection of claims 1-10 and 18 under 35 U.S.C. §103(a) as being obvious over Lu in view of Tang - Claim 1 is representative.

(3) Rejection of claims 13, 15, 18-26 and 28-39 under 35 U.S.C. §103(a) as being obvious over Tsu in view of Tang - Claim 13 is representative.

ARGUMENTS

In the ensuing discussion, the basis of patentability of the representative claim over the cited reference(s) will be set forth for each of the grounds of rejection identified in the preceding two sections ("ISSUES" and "GROUPING OF CLAIMS," respectively).

(1) Patentability of 1-8, 11-12, 14 and 16-17 under 35 U.S.C. §102(e) over Tsu - Claim 1 is representative

Claim 1 recites a microelectronic structure comprising, *inter alia*,

> **"at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof;**
>
> **at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al"**

The Examiner has incorrectly rejected claim 1, and claims 2-8, 11-12, 14, 16 and 17 dependent thereunder, on §102(e) grounds based on Tsu.

Specifically, the Examiner has mischaracterized Tsu on pages 2-3 of the May 19, 2003 Office Action, citing Tsu as disclosing, *inter alia*,

> **"at least one metal layer 20 in contact with the conductive barrier layer 22, wherein the metal layer 20 comprises metal or metal alloy including a material selected from the group consisting of Al, column 4 line 27, wherein at least one conductive barrier layer 22 is between at least one layer of high dielectric constant material 16 and at least one metal layer 20"**
>
> (Office Action, paragraph bridging pages 2 and 3)

In fact, layer 20 of Tsu is a silicide layer.

See Tsu at column 4, line 26 ("a silicide layer"); column 4, line 66 ("the silicide **20**"); column 6, line 18 ("metal silicide **20**"); column 6, line 24 ("metal silicide layer **20**"); etc.

A silicide is a silicon compound.

Silicon is NOT a metal - silicon is a semiconductor.

Tsu clearly recognizes the distinction between metals *per se*, and silicides. The layer 20 is described by Tsu as being formed of various silicide materials, including "aluminum silicide ($AlSi_x$)" (column 4, line 27 of Tsu) and "metal alloy silicides" (column 4, line 29 of Tsu).

The nomenclature of the latter species ("metal alloy silicides") clearly evidences that "metal alloy silicides" are different from "metal alloys" per se - the metal alloy silicides contain metals in the *ionic form as covalently bonded with silicon*, while metal alloys contain homogeneous mixtures or solid solutions of two or more metals in the *elemental form without covalent bonding*.

Therefore, **the metal silicide layer 20 disclosed by Tsu is different from the "at least one metal layer" required by Appellants' claimed invention**.

The application clearly describes metal electrodes in integrated circuit memory cells or other electronic devices - indeed, the title of the application, "Barrier Structures for Integration of High K Oxides With Cu and Al Electrodes," makes clear that the metalization referred to in the claims as constituting "at least one metal layer" is the electrode component of the recited microelectronic structure.

In this respect, see also the specification at page 4, line 12 ("**aluminum and copper have come into usage as alternative electrode materials**") and at page 5, lines 14-16 ("**the present invention therefore relates to use of various barrier layers between the complex metal oxides of high dielectric constant and the Cu or Al electrodes, to avoid the above-discussed problems**").

The Examiner's interpretation of "metal alloy" as being open to the inclusion of all materials other than those recited in the claim - e.g., wood, air, water, gas, etc - is a logical absurdity that is inconsistent with (i) the plain and simple recital of "at least one metal layer" and (ii) the clear and unambiguous meaning of such term as understood by those skilled in the art from a reading of Appellants' disclosure and claims.

A metal layer, simply stated, is a metal layer - it is not a metal silicide.

It is elemental patent law that the claims are construed and interpreted in light of the specification. See ***Markman v. Westview Instruments, Inc.***, 52 F.3d 967, 979 (Fed.Cir.1995) (en

banc), aff'd, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996) ("Claims must be read in light of the patent specification. ")

Further, it is old and well-established law that a claim to a composition comprising ingredients cited in the claim does not necessarily leave the claim open for inclusion of predominant amounts of unspecified ingredients or in such proportions to have an adverse effect on the basic composition. See ***Ex parte Fitzpatrick*** (Pat.Off.Bd.App. 1947), 82 USPQ 59 and ***Ex parte Geemzki*** (Pat.Off.Bd.App. 1948), 82 USPQ 120. In this respect, it is to be noted that the replacement of a substantial amount of metal with (semiconductor) silicon in the electrode as proposed by the Examiner (for this is the net result of using Tsu's silicide composition as "the metal layer") would have a severe adverse effect on the resulting layer, precluding its proper performance as an electrode.

It therefore is clear that **the metal silicide layer 20 disclosed by Tsu does not in any manner teach or suggest the "at least one metal layer" as required by Appellants' claimed invention**.

Tsu in his claim 7 discloses the step of "patterning **a layer of a metal** to form the patterned base eletrode," wherein a conductive nitride layer can be subsequently formed thereon via reaction with a nitrogen-bearing agent (see Tsu's claim 1, from which claim 7 of Tsu depends). Claim 8 of Tsu discloses that the metal for forming the base electrode is selected from the group consisting of tungsten (W), titanium (Ti), tantalum (Ta), zirconium (Zr), ruthenium (Ru), and molybdenum (Mo).

However, nothing in Tsu teaches or suggests that the metal layer upon which the conductive nitride layer is formed may comprise metals such as Cu, Al, or alloys thereof.

Tsu further discloses that the top electrode 14 can comprise any conductive material such as aluminum, copper, etc. (see Tsu, column 5, lines 23-24 and 27-28).

However, such top electrode 14 is formed directly over the dielectric layer 16 and is not in contact with any conductive barrier layer (see Tsu, column 3, lines 38-40 and Figures 2A-C).

Tsu therefore fails to provide any derivative basis for "**at least one metal layer**" comprising "**metal or metal alloy including a material selected from the group consisting of Cu and Al**" that is **in contact with a conductive barrier layer**, as required by Appellants' claim 1, and (by virtue of their dependence from claim 1) claims 2-8, 11-12, 14 and 16-17.

For the foregoing reasons, the Examiner's rejection of claims 1, 2-8, 11-12, 14 and 16-17 under 35 U.S.C. §102 (e) on the basis of Tsu is improper.

(2) Patentability of claims 1-10 and 18 under 35 U.S.C. §103(a) over Lu in view of Tang - Claim 1 is representative.

Concerning the Examiner's rejection of claims 1-10 and 18 based on Lu in view of Tang, Lu has been cited for disclosing a microelectronic structure featuring a TiN barrier layer between a metal layer (of aluminum or copper) and a high dielectric constant material, with Tang being cited as a secondary reference as allegedly disclosing that TiAlN can be used to replace TiN, the Examiner referring to column 9, lines 26-29 of Tang and stating that

> **"it would have been obvious to one of ordinary skill in the art to replace barrier layer 2/22 of Lu with Tang conductive barrier, because such material substitution would have been considered a mere substitution of art-recognized equivalent values" (May 19, 2003 Office Action, page 4).**

The Examiner's proposed basis for substituting TiAlN from Tang for TiN in Lu is illogical, as is apparent from the entire text of column 9, lines 26-29 of Tang, which the Examiner has cited in support of the rejection:

> **"In all of the preferred embodiments the <u>silicon diffusion barrier</u> alternatively could be made of TiAlN, W_2N, TaN, and so forth intead [sic - "instead" apparently intended] of the example TiN"**
>
> (emphasis added; Tang, column 9, lines 26-29)

This teaching has reference to the preceding disclosure in Tang, at column 8, lines 11-13:

> **"A conductive silicon diffusion barrier may be used on top of polysilicon-filled vias as TiN in FIG. 1a to avoid Ir-polysilicon interactions"** (Tang, column 8, lines 11-13)

Thus, the teachings in Tang that the Examiner has cited as a basis for rejecting claims 1-10 and 18 are directed to *barriers between polysilicon and iridium*, and **<u>there is therefore no basis for modifying Lu in a way that would yield TiAlN between a high dielectric constant material layer and a copper or aluminum layer, as in Appellants' claimed invention</u>**.

Further, Lu's teachings are specific to the use of TiN, $TiSi_xN_y$ or TiN_xB_y (see column 4, lines 32-36 of Lu) to form thin film diffusion barriers that are characterized by Lu as providing "lower resistivity" (Lu, at column 4, line 46) and "low contact/via resistance" (Lu, at column 4, lines 48-49), as well as "higher purity, density, and stability of the films formed by the instant invention" (Lu, at column 2, lines 17-18) - **<u>all suggestive of superior electrical performance</u>**. **<u>There is therefore no reason why one would change the specific barrier layer compositions taught by Lu, and risk the loss of such performance advantages</u>**. Additionally, the barrier cited in Tang is disposed between polysilicon and iridium, **<u>neither of which is a high dielectric constant</u>**

material. Accordingly, **there is no combination of Lu and Tang that yields the structure of Appellants' claimed invention**.

In sum, there is no basis in Lu or Tang for changing Lu's thin film structure in the manner proposed by the Examiner, and no basis in the aggregate disclosures of such references for deriving the Appellants' claimed invention.

In the September 11, 2003 Advisory Action, the Examiner has taken the position that the Tang reference justifies using TiAlN in place of Lu's TiN, as equivalents, and the Examiner has stated that "substitution of equivalent requires no express motivation as long as the prior art recognizes the equivalency."

The prior art, however, has NOT held that TiN = TiAlN as a general purpose diffusion barrier.

To the contrary, Tang has proposed TiAlN as a **SPECIFIC BARRIER MATERIAL** for a **SPECIFIC BARRIER APPLICATION** requiring that the TiAlN constitute a barrier **BETWEEN SPECIFIC ADJACENT MATERIALS**, namely, polysilicon and iridium.

This is apparent from Tang's express teachings, at column 8, lines 11-13:

> **"A conductive silicon diffusion barrier may be used on top of polysilicon-filled vias as TiN in FIG. 1a to avoid Ir-polysilicon interactions"**
>
> (emphasis added; Tang, col. 8, lines 11-13)

Lu has no such polysilicon/iridium structure or diffusional problems.

Since Tang has a **different material composition**, and a **different microelectronic device architecture**, and since Lu very clearly teaches **ONLY the use of TiN, $TiSi_xN_y$ or TiN_xB_y** (see column 4, lines 32-36 of Lu) to form thin film diffusion barriers with "**lower resistivity**" (column 4, line 46 of Lu), "**low contact/via resistance**" (column 4, lines 48-49 of Lu), and "**higher purity, density, and stability … films**" (column 2, lines 17-18 of Lu), the question that arises is,

> **"Why would one take Lu's very specific barrier compositions that are expressly stated to provide superior properties and performance advantages, and simply discard them, in favor of a substitution (from Tang) of a different material, taken from a different structure that involves different diffusional issues?"**

The Examiner has not answered this question, but instead has taken a position that one barrier material is interchangeable with any other barrier material, for any purpose, regardless of the types of materials and diffusional species involved.

This is inconsistent with the applicable law.

In any obviousness determination based on combination of two or more references, there must be some suggestion or motivation to combine the references, in the teachings of the references, or from the ordinary knowledge of persons skilled in the art, or from the nature of the problem to be solved. The operative question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. See ***WMS Gaming, Inc. v. International Game Technology***, 184 F.3d 1339, 1355 (Fed.Cir. 1999) and ***B.F. Goodrich Co. v. Aircraft Braking Systems Corp.***, 72 F.3d 1577, 1582 (Fed.Cir. 1996) ("When obviousness is based on a particular prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference.")

To establish a *prima facie* case of obviousness based on a combination of the content of various references, there must be some teaching, suggestion or motivation in the prior art to make the specific combination that is present in the applicant's claimed invention. See ***In re Dance***, 160 F.3d 1339, 1342 (Fed. Cir. 1998) and ***In re Oetiker***, 977 F.2d 1443, 1445 (Fed.Cir.1992).

Tang's teachings are directed to barriers between polysilicon and iridium. There is no such structure in Lu, and no basis in Lu and/or Tang for importing the polysilicon and iridium barrier layer of Tang into the non-analogous structure of Lu.

The teachings of Tang and Lu **in the context of their overall disclosures of different materials and different device architectures** are relevant to the issue of their combinability, and must be considered. See ***W.L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) (a prior art reference must be considered in its entirety, as a whole, including portions that would lead away from the claimed invention).

One cannot select isolated features out of context, and re-implement them in a manner inconsistent with the contextual disclosure of their source references, simply by declaring such isolated features interchangeable for all purposes[2]. Rather than providing a proper basis for obviousness, such an approach shows only a hindsight attempt to reconstruct the Appellants' invention. The law is clear in this respect. Obviousness cannot be established by hindsight combination to produce the claimed invention. ***In re Gorman***, 933 F.2d 982, 986, 18 USPQ2d 1885, 1888 (Fed.Cir.1991).

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[2] Just because an apple is a recognized equivalent to an orange *as a fruit* does not mean that oranges can be used to make applesauce.

Tang and Lu provide no basis for utilizing TiAlN as a barrier material between a high dielectric constant material layer and a copper or aluminum layer, as in Applicant's claimed invention.

For all the foregoing reasons, the microelectronic structure as recited in claims 1-10 and 18 is patentably distinguished over Lu in view of Tang, and the Examiner's rejections of such claims based on such cited references are incorrect.

(3) Patentability of claims 13, 15, 18-26 and 28-39 under 35 U.S.C. §103(a) over Tsu in view of Tang - Claim 13 is representative

The rejections of dependent claims 13, 15, 18-26 and 28-39 based on Tsu in view of Tang suffer from the same deficiencies as noted in the discussion hereinabove of Tsu as a §102(e) reference in relation to Appellants' claim 1, from which each of claims 13, 15, 18-26 and 28-39 directly or indirectly depends.

Accordingly, all of the Examiner's proposed respective modifications of Tsu, e.g., to incorporate various barrier layer materials of Tang, to use multiple barrier layers as in Tang, etc., do not change the fact that the resulting structures in every case would still have the silicide layer of Tsu, and would lack the "at least one metal layer" required by Appellants' broad claim 1, from which each of claims 13, 15, 18-26 and 28-39 directly or indirectly depends.

Claims 13, 15, 18-26 and 28-39 therefore are patentable over Tsu in view of Tang, and the §103 (a) rejections of such claims based on the Tsu and Tang references are incorrect.

CONCLUSION

Based on the foregoing arguments and cited legal precedent, it is respectfully requested that the Board of Patent Appeals and Interferences reverse the decision of the Examiner finally rejecting claims 1-26 and 28-39, consistent with the patentability of such claims over the cited prior art.

FEE PAYABLE FOR FILING OF THIS APPEAL BRIEF

The Office is hereby authorized to charge the $330.00 fee payable for filing of this Appeal Brief under 37 CFR 1.17(c) to the credit card as specified in the Credit Card Payment Form enclosed herewith.

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APPENDIX A

Pending Claims 1-39

1. A microelectronic structure comprising:

at least one layer of high dielectric constant material;

at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof;

at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al;

wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;

wherein when said material of said at least one metal layer is Al, said at least one material of said conductive barrier layer is not Ir or IrO_2.

2. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises at least one material selected from the group consisting of TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, and NbAlN.

3. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

4. A microelectronic structure according to claim 1, wherein said metal layer comprises Cu or Cu alloy.

5. A microelectronic structure according to claim 1, wherein said metal layer comprises Al or Al alloy.

6. A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises a complex metal oxide selected from the group consisting of $SrBi_2Ta_2O_9$ (SBT), $(Ba,Sr)TiO_3$ (BST), $BiTaO_4$ (BT), and $Pb(Zr,Ti)O_3$ (PZT).

7. A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises perovskite BST material.

8. A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises amorphous BST material.

9. A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 1nm to about 100nm.

10. A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 5nm to about 20nm.

11. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Pt.

12. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ir.

13. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises IrO_2.

14. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ru.

15. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises RuO_2.

16. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

17. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TaN.

18. A microelectronic structure according to claim 1, comprising a first conductive barrier layer and a second conductive barrier layer, wherein the first conductive barrier layer is in contact with the layer of high dielectric constant material, and the second conductive barrier layer overlies said first conductive barrier layer and is in contact with the metal layer.

19. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises IrO_2.

20. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises TiAlN.

21. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises Ir.

22. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises IrO_2.

23. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises TiAlN.

24. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises Ir.

25. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises TiAlN.

26. A microelectronic structure according to claim 1, comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer.

27. A microelectronic structure comprising:

at least one layer of high dielectric constant material;

at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof;

at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu or and Al;

wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;

wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;

wherein when said material of said at least one metal layer is Al, said at least one material of said conductive barrier layer is not Ir or IrO_2;

comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer,

wherein said first conductive barrier layer comprises IrO_2, said second conductive barrier layer comprises Ir_2O_3, and said third conductive barrier layer comprises Ir.

28. A microelectronic structure according to claim 1, comprising:

at least one layer of perovskite BST material;

a first conductive barrier layer in contact with the layer of perovskite BST material, and comprising Pt;

a second conductive barrier layer overlaying said first conductive barrier layer, and comprising Ir; and

at least one metal layer in contact with said second conductive barrier layer, comprising Cu or Cu alloy.

29. A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous BST material;

a conductive barrier layer in contact with the layer of amorphous BST material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

30. A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous SBT material;

a conductive barrier layer in contact with the layer of amorphous SBT material, comprising at least one material selected from the group consisting of Ir, Ru, TaN and TiAlN;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

31. A microelectronic structure according to claim 1, comprising:

at least one layer of PZT material;

a conductive barrier layer in contact with the layer of PZT material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

32. A microelectronic structure according to claim 1, comprising a capacitor structure selected from the group consisting of stack capacitors and trench capacitors.

33. A microelectronic structure according to claim 1, comprising a memory cell integrated circuit structure.

34. A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a non-volatile memory cell integrated circuit structure.

35. A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a dynamic random access memory cell integrated circuit structure.

36. A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises a decoupling circuit.

37. A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an impedance matching circuit.

38. A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an analog circuit component.

39. A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an active circuit element selected from the group consisting of electrically tunable capacitor, sensor, and microelectromechanical machine (MEMS).

BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE
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Expires: August 28, 2004

Harry I. Moatz
Director of Enrollment and Discipline

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re United States Patent Application of:		**Docket No.:**	**2771-497 (7486)**
Applicant:	**STAUF, Gregory T., et al.**	**Examiner:**	**Thao X. LE**
Application No.:	**09/681,609**	**Art Group:**	**2814**
Date Filed:	**May 8, 2001**	**Confirm. No.:**	**8601**
Title:	**BARRIER STRUCTURES FOR INTEGRATION OF HIGH K OXIDES WITH Cu AND Al ELECTRODES**	**Customer Number**	**25559**

EXPRESS MAIL CERTIFICATE

I hereby certify that I am mailing the attached documents to the Commissioner for Patents on January 20, 2004, in a postage prepaid envelope addressed to Mail Stop Appeal Brief–Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, and Express Mailed under the provisions of 37 CFR 1.10.

Candace White

CandaceWhite

January 20, 2004

Date

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APPEAL BRIEF
IN U.S. PATENT APPLICATION NO. 09/681,609

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This Appeal Brief is filed in support of the appeal initiated by Notice of Appeal filed November 18, 2003 in U.S. Patent Application No. 09/681,609, appealing from the final rejection of claims 1-39 in the May 19, 2003 Office Action.

This Appeal Brief is submitted in triplicate copies.

An oral hearing is not requested.

REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Technology Materials, Inc., 7 Commerce Drive, Danbury, CT 06810. Such party is the owner of the invention and patent rights of the present application by virtue of an assignment from the inventors Gregory T. Stauf, Bryan C. Hendrix, Jeffrey F. Roeder, and Ing-Shin Chen, as recorded in the assignment records of the U.S. Patent and Trademark Office on July 26, 2001 at Reel 012012, Frame 0409 (3 pages).

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellants, appellants' legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-39 are pending in the present application and are the subject of this appeal.

Claims 1-26 and 28-39 has been finally rejected in the May 19, 2003 Office Action. Claim 27 was found to prospectably allowable if re-written in independent form and was rewritten in the Amendment filed on November 18, 2003.

A copy of the appealed claims 1-39 is attached in **Appendix A** hereof.

STATUS OF AMENDMENTS

No amendments have been made to the claims 1-26 and 28-39 subsequent to the issue of the May 19, 2003 Office Action finally rejecting such claims.

The prospectably allowable claim 27 was first rewritten into independent form in a Response filed on August 19, 2003. The Examiner denied entry of the August 19, 2003 Response, on the basis that claim 27 was not rewritten in proper form, i.e., it failed to incorporate all limitations of the base and intervening claims therein.

In an Amendment subsequently filed on November 18, 2003, claim 27 was for the second time rewritten into independent form, by incorporating all limitations of the base and intervening claims therein, consistent with the Examiner's requirement. However, to this date, the Appellants have not yet received any communication from the Office regarding either entry of or refusal to enter the November 18, 2003 Amendment.[1]

Because the November 18, 2003 Amendment complies with the Examiner's requirement and is enterable udner 37 C.F.R. 1.116 (b), claim 27 in the attached listing of claims is set forth in its rewritten independent form as amended in the November 18, 2003 Amendment.

SUMMARY OF THE INVENTION

Appellants' claimed invention is a microelectronic structure comprising at least one conductive barrier layer between a layer of high dielectric constant material and a metal layer comprising Cu or Al, which can function as a Cu or Al electrode.

---

[1] A telephone call was made to Examiner Le on January 13, 2004 concerning the status of the November 18, 2003 Amendment; Examiner Le stated that the November 18, 2003 Amendment had not reached the Examiner until January 5, 2004 and has not yet been reviewed by the Examiner.

Complex metal oxides such as $SrBi_2Ta_2O_9$ (SBT), $(Ba,Sr)TiO_3$ (BST), and $Pb(Zr,Ti)O_3$(PZT), which are characterized by high dielectric constants, are particularly suitable for forming integrated capacitors of high capacitance.

However, usage of such high dielectric constant materials require electrodes made from noble metals, noble metal alloys, or noble metal oxides, etc., which are expensive and difficult to process. They are further disadvantaged by their relatively low conductivity.

Aluminum and copper electrodes, on the other hand, not only are cheap and easy to process, but also have excellent conductivity. However, aluminum and copper electrodes are vulnerable to oxidization and are difficult to use in combination with high dielectric constant metal oxides.

Appellants' claimed invention solves the above-described problem by providing a conductive barrier structure between the high dielectric constant material and the aluminum or copper electrode.

Specifically, the claimed microelectronic structure, as recited by claim 1 of the present application, comprises:

> at least one layer of high dielectric constant material (see page 6, lines 11-17 of the instant specification);
>
> at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from

the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof (see page 7, lines 9-14 and page 13, lines 1-18 of the instant specification);

at least one metal layer in contact with the conductive barrier layer, wherein such metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al, with the limitation that when the at least one metal layer material is Al, the at least one conductive barrier material is not Ir or IrO_2 (see page 6, lines 8-10 and page 7, lines 15-19 of the instant specification); and

wherein the at least one conductive barrier layer is between the at least one layer of high dielectric constant material and the at least one metal layer (see page 6, lines 9-11 of the instant specification).

The at least one metal layer of Appellants' claimed invention thus provide a metal electrode that comprises Cu, Cu alloy, Al, Al alloy, or other combinations of metals that contain Cu and/or Al (see page 8, last paragraph, and page 9, first paragraph of the instant specification).

The conductive barrier structure of the present invention may comprise two or three barrier layers, as recited in claims 18-26 and 28 of the present application and disclosed on page 8, lines 3-6; page 9, lines 4-18; and page 10, lines 1-5 of the instant specification).

Further, Appellant's claimed invention encompasses various conductive barrier structures that are particularly suitable for protecting a metal layer that comprises Cu or Cu alloy from high

dielectric constant BST, SBT, BT, or PZT material layers, as recited in claims 28-31 and disclosed on pages 10-12 of the instant specification.

Appellants' claimed invention therefore provides effective conductive barrier structures for protecting Cu- and/or Al-containing metal electrodes from high dielectric constant material layers.

ISSUES

The issue presented in this appeal are:

(1) Whether claims 1-8, 11-12, 14 and 16-17 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Tsu et al. USP 6,294,420 (hereafter "Tsu");

(2) Whether claims 1-10 and 18 are unpatentable under 35 U.S.C. §103(a) as being obvious over Lu et al. USP 6,365,517 (hereafter "Lu") in view of Tang et al. USP 6,462,931 (hereafter "Tang"); and

(3) Whether claims 13, 15, 18-26 and 28-39 are unpatentable under 35 U.S.C. §103(a) as being obvious over Tsu in view of Tang.

GROUPING OF CLAIMS

For each ground of rejection set out in the preceding section ("ISSUES"), the representative claim is identified below.

(1) Rejection of claims 1-8, 11-12, 14 and 16-17 under 35 U.S.C. §102(e) as being anticipated by Tsu - Claim 1 is representative.

(2) Rejection of claims 1-10 and 18 under 35 U.S.C. §103(a) as being obvious over Lu in view of Tang - Claim 1 is representative.

(3) Rejection of claims 13, 15, 18-26 and 28-39 under 35 U.S.C. §103(a) as being obvious over Tsu in view of Tang - Claim 13 is representative.

ARGUMENTS

In the ensuing discussion, the basis of patentability of the representative claim over the cited reference(s) will be set forth for each of the grounds of rejection identified in the preceding two sections ("ISSUES" and "GROUPING OF CLAIMS," respectively).

(1) Patentability of 1-8, 11-12, 14 and 16-17 under 35 U.S.C. §102(e) over Tsu - Claim 1 is representative

Claim 1 recites a microelectronic structure comprising, *inter alia*,

> **"at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof;**
>
> **at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al"**

The Examiner has incorrectly rejected claim 1, and claims 2-8, 11-12, 14, 16 and 17 dependent thereunder, on §102(e) grounds based on Tsu.

Specifically, the Examiner has mischaracterized Tsu on pages 2-3 of the May 19, 2003 Office Action, citing Tsu as disclosing, *inter alia*,

> **"at least one metal layer 20 in contact with the conductive barrier layer 22, wherein the metal layer 20 comprises metal or metal alloy including a material selected from the group consisting of Al, column 4 line 27, wherein at least one conductive barrier layer 22 is between at least one layer of high dielectric constant material 16 and at least one metal layer 20"**
>
> (Office Action, paragraph bridging pages 2 and 3)

In fact, layer 20 of Tsu is a silicide layer.

See Tsu at column 4, line 26 ("a silicide layer"); column 4, line 66 ("the silicide **20**"); column 6, line 18 ("metal silicide **20**"); column 6, line 24 ("metal silicide layer **20**"); etc.

A silicide is a silicon compound.

Silicon is NOT a metal - silicon is a semiconductor.

Tsu clearly recognizes the distinction between metals *per se*, and silicides. The layer 20 is described by Tsu as being formed of various silicide materials, including "aluminum silicide ($AlSi_x$)" (column 4, line 27 of Tsu) and "metal alloy silicides" (column 4, line 29 of Tsu).

The nomenclature of the latter species ("metal alloy silicides") clearly evidences that "metal alloy silicides" are different from "metal alloys" per se - the metal alloy silicides contain metals in the *ionic form as covalently bonded with silicon*, while metal alloys contain homogeneous mixtures or solid solutions of two or more metals in the *elemental form without covalent bonding*.

Therefore, **the metal silicide layer 20 disclosed by Tsu is different from the "at least one metal layer" required by Appellants' claimed invention**.

The application clearly describes metal electrodes in integrated circuit memory cells or other electronic devices - indeed, the title of the application, "Barrier Structures for Integration of High K Oxides With Cu and Al Electrodes," makes clear that the metalization referred to in the claims as constituting "at least one metal layer" is the electrode component of the recited microelectronic structure.

In this respect, see also the specification at page 4, line 12 ("**aluminum and copper have come into usage as alternative electrode materials**") and at page 5, lines 14-16 ("**the present invention therefore relates to use of various barrier layers between the complex metal oxides of high dielectric constant and the Cu or Al electrodes, to avoid the above-discussed problems**").

The Examiner's interpretation of "metal alloy" as being open to the inclusion of all materials other than those recited in the claim - e.g., wood, air, water, gas, etc - is a logical absurdity that is inconsistent with (i) the plain and simple recital of "at least one metal layer" and (ii) the clear and unambiguous meaning of such term as understood by those skilled in the art from a reading of Appellants' disclosure and claims.

A metal layer, simply stated, is a metal layer - it is not a metal silicide.

It is elemental patent law that the claims are construed and interpreted in light of the specification. See ***Markman v. Westview Instruments, Inc.***, 52 F.3d 967, 979 (Fed.Cir.1995) (en

banc), aff'd, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996) ("Claims must be read in light of the patent specification. ")

Further, it is old and well-established law that a claim to a composition comprising ingredients cited in the claim does not necessarily leave the claim open for inclusion of predominant amounts of unspecified ingredients or in such proportions to have an adverse effect on the basic composition. See ***Ex parte Fitzpatrick*** (Pat.Off.Bd.App. 1947), 82 USPQ 59 and ***Ex parte Geemzki*** (Pat.Off.Bd.App. 1948), 82 USPQ 120. In this respect, it is to be noted that the replacement of a substantial amount of metal with (semiconductor) silicon in the electrode as proposed by the Examiner (for this is the net result of using Tsu's silicide composition as "the metal layer") would have a severe adverse effect on the resulting layer, precluding its proper performance as an electrode.

It therefore is clear that **the metal silicide layer 20 disclosed by Tsu does not in any manner teach or suggest the "at least one metal layer" as required by Appellants' claimed invention**.

Tsu in his claim 7 discloses the step of "patterning **a layer of a metal** to form the patterned base eletrode," wherein a conductive nitride layer can be subsequently formed thereon via reaction with a nitrogen-bearing agent (see Tsu's claim 1, from which claim 7 of Tsu depends). Claim 8 of Tsu discloses that the metal for forming the base electrode is selected from the group consisting of tungsten (W), titanium (Ti), tantalum (Ta), zirconium (Zr), ruthenium (Ru), and molybdenum (Mo).

However, nothing in Tsu teaches or suggests that the metal layer upon which the conductive nitride layer is formed may comprise metals such as Cu, Al, or alloys thereof.

Tsu further discloses that the top electrode 14 can comprise any conductive material such as aluminum, copper, etc. (see Tsu, column 5, lines 23-24 and 27-28).

However, such top electrode 14 is formed directly over the dielectric layer 16 and is not in contact with any conductive barrier layer (see Tsu, column 3, lines 38-40 and Figures 2A-C).

Tsu therefore fails to provide any derivative basis for "**at least one metal layer**" comprising "**metal or metal alloy including a material selected from the group consisting of Cu and Al**" that is **in contact with a conductive barrier layer**, as required by Appellants' claim 1, and (by virtue of their dependence from claim 1) claims 2-8, 11-12, 14 and 16-17.

For the foregoing reasons, the Examiner's rejection of claims 1, 2-8, 11-12, 14 and 16-17 under 35 U.S.C. §102 (e) on the basis of Tsu is improper.

(2) Patentability of claims 1-10 and 18 under 35 U.S.C. §103(a) over Lu in view of Tang - Claim 1 is representative.

Concerning the Examiner's rejection of claims 1-10 and 18 based on Lu in view of Tang, Lu has been cited for disclosing a microelectronic structure featuring a TiN barrier layer between a metal layer (of aluminum or copper) and a high dielectric constant material, with Tang being cited as a secondary reference as allegedly disclosing that TiAlN can be used to replace TiN, the Examiner referring to column 9, lines 26-29 of Tang and stating that

> **"it would have been obvious to one of ordinary skill in the art to replace barrier layer 2/22 of Lu with Tang conductive barrier, because such material substitution would have been considered a mere substitution of art-recognized equivalent values" (May 19, 2003 Office Action, page 4).**

The Examiner's proposed basis for substituting TiAlN from Tang for TiN in Lu is illogical, as is apparent from the entire text of column 9, lines 26-29 of Tang, which the Examiner has cited in support of the rejection:

> **"In all of the preferred embodiments the <u>silicon diffusion barrier</u> alternatively could be made of TiAlN, W_2N, TaN, and so forth intead [sic - "instead" apparently intended] of the example TiN"**
>
> (emphasis added; Tang, column 9, lines 26-29)

This teaching has reference to the preceding disclosure in Tang, at column 8, lines 11-13:

> **"A conductive silicon diffusion barrier may be used on top of polysilicon-filled vias as TiN in FIG. 1a to avoid Ir-polysilicon interactions"** (Tang, column 8, lines 11-13)

Thus, the teachings in Tang that the Examiner has cited as a basis for rejecting claims 1-10 and 18 are directed to *barriers between polysilicon and iridium*, and **<u>there is therefore no basis for modifying Lu in a way that would yield TiAlN between a high dielectric constant material layer and a copper or aluminum layer, as in Appellants' claimed invention</u>**.

Further, Lu's teachings are specific to the use of TiN, $TiSi_xN_y$ or TiN_xB_y (see column 4, lines 32-36 of Lu) to form thin film diffusion barriers that are characterized by Lu as providing "lower resistivity" (Lu, at column 4, line 46) and "low contact/via resistance" (Lu, at column 4, lines 48-49), as well as "higher purity, density, and stability of the films formed by the instant invention" (Lu, at column 2, lines 17-18) - **<u>all suggestive of superior electrical performance</u>**. **<u>There is therefore no reason why one would change the specific barrier layer compositions taught by Lu, and risk the loss of such performance advantages</u>**. Additionally, the barrier cited in Tang is disposed between polysilicon and iridium, **<u>neither of which is a high dielectric constant</u>**

material. Accordingly, **there is no combination of Lu and Tang that yields the structure of Appellants' claimed invention**.

In sum, there is no basis in Lu or Tang for changing Lu's thin film structure in the manner proposed by the Examiner, and no basis in the aggregate disclosures of such references for deriving the Appellants' claimed invention.

In the September 11, 2003 Advisory Action, the Examiner has taken the position that the Tang reference justifies using TiAlN in place of Lu's TiN, as equivalents, and the Examiner has stated that "substitution of equivalent requires no express motivation as long as the prior art recognizes the equivalency."

The prior art, however, has NOT held that TiN = TiAlN as a general purpose diffusion barrier.

To the contrary, Tang has proposed TiAlN as a **SPECIFIC BARRIER MATERIAL** for a **SPECIFIC BARRIER APPLICATION** requiring that the TiAlN constitute a barrier **BETWEEN SPECIFIC ADJACENT MATERIALS**, namely, polysilicon and iridium.

This is apparent from Tang's express teachings, at column 8, lines 11-13:

> **"A conductive silicon diffusion barrier may be used on top of polysilicon-filled vias as TiN in FIG. 1a to avoid Ir-polysilicon interactions"**
>
> (emphasis added; Tang, col. 8, lines 11-13)

Lu has no such polysilicon/iridium structure or diffusional problems.

Since Tang has a **different material composition**, and a **different microelectronic device architecture**, and since Lu very clearly teaches **ONLY the use of TiN, $TiSi_xN_y$ or TiN_xB_y** (see column 4, lines 32-36 of Lu) to form thin film diffusion barriers with "**lower resistivity**" (column 4, line 46 of Lu), "**low contact/via resistance**" (column 4, lines 48-49 of Lu), and "**higher purity, density, and stability … films**" (column 2, lines 17-18 of Lu), the question that arises is,

> **"Why would one take Lu's very specific barrier compositions that are expressly stated to provide superior properties and performance advantages, and simply discard them, in favor of a substitution (from Tang) of a different material, taken from a different structure that involves different diffusional issues?"**

The Examiner has not answered this question, but instead has taken a position that one barrier material is interchangeable with any other barrier material, for any purpose, regardless of the types of materials and diffusional species involved.

This is inconsistent with the applicable law.

In any obviousness determination based on combination of two or more references, there must be some suggestion or motivation to combine the references, in the teachings of the references, or from the ordinary knowledge of persons skilled in the art, or from the nature of the problem to be solved. The operative question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. See ***WMS Gaming, Inc. v. International Game Technology***, 184 F.3d 1339, 1355 (Fed.Cir. 1999) and ***B.F. Goodrich Co. v. Aircraft Braking Systems Corp.***, 72 F.3d 1577, 1582 (Fed.Cir. 1996) ("When obviousness is based on a particular prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference.")

To establish a *prima facie* case of obviousness based on a combination of the content of various references, there must be some teaching, suggestion or motivation in the prior art to make the specific combination that is present in the applicant's claimed invention. See ***In re Dance***, 160 F.3d 1339, 1342 (Fed. Cir. 1998) and ***In re Oetiker***, 977 F.2d 1443, 1445 (Fed.Cir.1992).

Tang's teachings are directed to barriers between polysilicon and iridium. There is no such structure in Lu, and no basis in Lu and/or Tang for importing the polysilicon and iridium barrier layer of Tang into the non-analogous structure of Lu.

The teachings of Tang and Lu **in the context of their overall disclosures of different materials and different device architectures** are relevant to the issue of their combinability, and must be considered. See ***W.L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) (a prior art reference must be considered in its entirety, as a whole, including portions that would lead away from the claimed invention).

One cannot select isolated features out of context, and re-implement them in a manner inconsistent with the contextual disclosure of their source references, simply by declaring such isolated features interchangeable for all purposes[2]. Rather than providing a proper basis for obviousness, such an approach shows only a hindsight attempt to reconstruct the Appellants' invention. The law is clear in this respect. Obviousness cannot be established by hindsight combination to produce the claimed invention. ***In re Gorman***, 933 F.2d 982, 986, 18 USPQ2d 1885, 1888 (Fed.Cir.1991).

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[2] Just because an apple is a recognized equivalent to an orange *as a fruit* does not mean that oranges can be used to make applesauce.

Tang and Lu provide no basis for utilizing TiAlN as a barrier material between a high dielectric constant material layer and a copper or aluminum layer, as in Applicant's claimed invention.

For all the foregoing reasons, the microelectronic structure as recited in claims 1-10 and 18 is patentably distinguished over Lu in view of Tang, and the Examiner's rejections of such claims based on such cited references are incorrect.

(3) Patentability of claims 13, 15, 18-26 and 28-39 under 35 U.S.C. §103(a) over Tsu in view of Tang - Claim 13 is representative

The rejections of dependent claims 13, 15, 18-26 and 28-39 based on Tsu in view of Tang suffer from the same deficiencies as noted in the discussion hereinabove of Tsu as a §102(e) reference in relation to Appellants' claim 1, from which each of claims 13, 15, 18-26 and 28-39 directly or indirectly depends.

Accordingly, all of the Examiner's proposed respective modifications of Tsu, e.g., to incorporate various barrier layer materials of Tang, to use multiple barrier layers as in Tang, etc., do not change the fact that the resulting structures in every case would still have the silicide layer of Tsu, and would lack the "at least one metal layer" required by Appellants' broad claim 1, from which each of claims 13, 15, 18-26 and 28-39 directly or indirectly depends.

Claims 13, 15, 18-26 and 28-39 therefore are patentable over Tsu in view of Tang, and the §103 (a) rejections of such claims based on the Tsu and Tang references are incorrect.

CONCLUSION

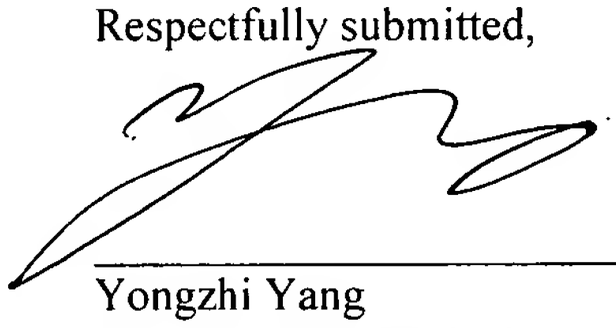
Based on the foregoing arguments and cited legal precedent, it is respectfully requested that the Board of Patent Appeals and Interferences reverse the decision of the Examiner finally rejecting claims 1-26 and 28-39, consistent with the patentability of such claims over the cited prior art.

FEE PAYABLE FOR FILING OF THIS APPEAL BRIEF

The Office is hereby authorized to charge the $330.00 fee payable for filing of this Appeal Brief under 37 CFR 1.17(c) to the credit card as specified in the Credit Card Payment Form enclosed herewith.

Authorization hereby is given to charge any additional fee or amount properly payable for the filing and entry of this Appeal Brief, and to credit any excess payment, to Deposit Account No. 08-3284 of Intellectual Property/Technology Law.

Respectfully submitted,



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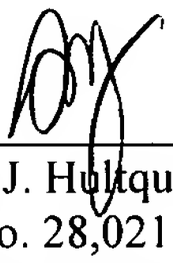

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APPENDIX A

Pending Claims 1-39

1. A microelectronic structure comprising:

at least one layer of high dielectric constant material;

at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof;

at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al;

wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;

wherein when said material of said at least one metal layer is Al, said at least one material of said conductive barrier layer is not Ir or IrO_2.

2. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises at least one material selected from the group consisting of TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, and NbAlN.

3. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

4. A microelectronic structure according to claim 1, wherein said metal layer comprises Cu or Cu alloy.

5. A microelectronic structure according to claim 1, wherein said metal layer comprises Al or Al alloy.

6. A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises a complex metal oxide selected from the group consisting of $SrBi_2Ta_2O_9$ (SBT), $(Ba,Sr)TiO_3$ (BST), $BiTaO_4$ (BT), and $Pb(Zr,Ti)O_3$ (PZT).

7. A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises perovskite BST material.

8. A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises amorphous BST material.

9. A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 1nm to about 100nm.

10. A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 5nm to about 20nm.

11. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Pt.

12. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ir.

13. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises IrO_2.

14. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ru.

15. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises RuO_2.

16. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

17. A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TaN.

18. A microelectronic structure according to claim 1, comprising a first conductive barrier layer and a second conductive barrier layer, wherein the first conductive barrier layer is in contact with the layer of high dielectric constant material, and the second conductive barrier layer overlies said first conductive barrier layer and is in contact with the metal layer.

19. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises IrO_2.

20. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises TiAlN.

21. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises Ir.

22. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises IrO_2.

23. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises TiAlN.

24. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises Ir.

25. A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises TiAlN.

26. A microelectronic structure according to claim 1, comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer.

27. A microelectronic structure comprising:

at least one layer of high dielectric constant material;

at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof;

at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu or and Al;

wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;

wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;

wherein when said material of said at least one metal layer is Al, said at least one material of said conductive barrier layer is not Ir or IrO_2;

comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer,

wherein said first conductive barrier layer comprises IrO_2, said second conductive barrier layer comprises Ir_2O_3, and said third conductive barrier layer comprises Ir.

28. A microelectronic structure according to claim 1, comprising:

at least one layer of perovskite BST material;

a first conductive barrier layer in contact with the layer of perovskite BST material, and comprising Pt;

a second conductive barrier layer overlaying said first conductive barrier layer, and comprising Ir; and

at least one metal layer in contact with said second conductive barrier layer, comprising Cu or Cu alloy.

29. A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous BST material;

a conductive barrier layer in contact with the layer of amorphous BST material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

30. A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous SBT material;

a conductive barrier layer in contact with the layer of amorphous SBT material, comprising at least one material selected from the group consisting of Ir, Ru, TaN and TiAlN;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

31. A microelectronic structure according to claim 1, comprising:

at least one layer of PZT material;

a conductive barrier layer in contact with the layer of PZT material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

32. A microelectronic structure according to claim 1, comprising a capacitor structure selected from the group consisting of stack capacitors and trench capacitors.

33. A microelectronic structure according to claim 1, comprising a memory cell integrated circuit structure.

34. A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a non-volatile memory cell integrated circuit structure.

35. A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a dynamic random access memory cell integrated circuit structure.

36. A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises a decoupling circuit.

37. A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an impedance matching circuit.

38. A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an analog circuit component.

39. A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an active circuit element selected from the group consisting of electrically tunable capacitor, sensor, and microelectromechanical machine (MEMS).

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